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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,848	12/21/2000	Vladislav Vashchenko	NSC1-H2000 (P04846)	4415

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/747,848	Applicant(s) VASHCHENKO ET AL.
	Examiner ori nadav	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-10 and 12-14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for a well region having a floating potential, as recited in claims 1 and 12.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5, 8, 10 and 12-13, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al. (5,939,767). Brown et al. teach in figure 27 and related text an ESD protection structure for use with RF frequency integrated circuits comprising: a P- epitaxial silicon semiconductor substrate; an N- well region having a floating potential disposed in the semiconductor substrate; a P+ first region disposed in the N-well region on the P- epitaxial silicon semiconductor substrate; an N+ second region (connected to Vrail) disposed in and on the P- epitaxial silicon semiconductor substrate and spaced apart from the P+ first region and the N-well region; and a shallow trench isolation region disposed in the P- epitaxial silicon semiconductor substrate between the P+ first region and the N+ second region, wherein the maximum dopant concentration of the semiconductor substrate is less than the maximum dopant concentration of the first region and the maximum dopant concentration of the well region is less than the maximum dopant concentration of the second region, and having a bottom contact to the semiconductor substrate.

Regarding claim 8, Brown et al. teach configuring the ESD device between an input/output line of an integrated circuit and GND.

5. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Wei et al. (5,843,813).

Wei et al. teach in figure 20 and related text an ESD protection structure formed in a P type semiconductor material 290 comprising an isolation region (the FOX region) formed in the semiconductor material, an N+ first region 256 formed in the semiconductor material, an N-well region 292 in the semiconductor material, contacting the isolation region, being spaced apart from the N+ first region 256, having a dopant concentration less than that of the first region, and not contacting an N+ region, a P+ second region 252 contacting the isolation region.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 6, 7 and 9, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al.

Regarding claim 4, Brown et al. teaches substantially the entire claimed structure, as applied to claims 1-3 above, except stating that the embodiment dopant concentration

of the semiconductor substrate is 5E15 atoms/cm3, the maximum dopant concentration of the well region is 2E17 atoms/cm3, the maximum dopant concentration of the first region is 5E20 atoms/cm3, the maximum dopant concentration of the second region is 5E20 atoms/cm3, and the P- epitaxial silicon layer has a dopant concentration no greater than 5E15 atoms/cm3.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use dopant concentration of the semiconductor substrate is 5E15 atoms/cm3, the maximum dopant concentration of the well region is 2E17 atoms/cm3, the maximum dopant concentration of the first region is 5E20 atoms/cm3, the maximum dopant concentration of the second region is 5E20 atoms/cm3, and the P- epitaxial silicon layer has a dopant concentration no greater than 5E15 atoms/cm3. in Brown et al.'s device, since it is within the skills of an artisan, subject to routine experimentation and optimization to adjust the dopant concentration of the first and second regions and the substrate. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this

principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 6, Brown et al. do not explicitly state that the semiconductor substrate of figure 27 is a P- epitaxial silicon semiconductor substrate. Brown et al. teach that the semiconductor substrate of the disclosed invention is a P- epitaxial silicon semiconductor substrate (column 16, line 47 and column 17, line 57 to column 18, line 8). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an epitaxial silicon semiconductor substrate in the embodiment of figure 27 of Brown et al.'s device in order to have more control over the thickness of the doped layer with a better quality material and in order to form the device as taught by Brown et al.

Regarding claim 9, Brown et al. do not teach using the device between a VDD line of the integrated circuit and a differential amplifier of the integrated circuit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to configure Brown et al.'s device between a VDD line of the integrated circuit and a differential amplifier of the integrated circuit in order to use the device in an application

which requires an ESD protection between a VDD line of the integrated circuit and a differential amplifier of the integrated circuit.

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al.

Wei et al. teach substantially the entire claimed structure, as applied to claim 15 above, except stating that the second region is connected to an electrical pad and the first region is connected to ground. Wei et al. teach in figure 18 a second region (source region of one transistor) connected to an electrical pad and a first region (drain region of a second transistor) connected to ground. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the second region to an electrical pad and the first region to ground in Wei et al.'s device in order to operate the device in its intended use.

Response to Arguments

9. Applicant argues that figure 8A of the present invention provides support for a well region having a floating potential.

Figure 8A of the present invention does not provide support for a well region having a floating potential. Figure 8A depicts a diode connected between an input pad

and a ground potential with no illustration of a floating well. In fact, the well region can not have a floating potential since the well is connected to an input pad potential and/or a ground potential.

10. The rest of applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM

(Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

December 9, 2002